## REMARKS

Claims 1-16 are pending in the application. Claims 1, 8 and 12 have been amended by way of the present amendment. Reconsideration is respectfully requested.

In the outstanding Office Action, claims 1-16 were rejected under 35 USC 103(a) as being unpatentable over U.S. Patent No. 6,356,990 (Aoki et al.) in view of U.S. Patent No. 5,920,888 (Shirotori et al.) and further in view of US Patent Application Publication No. 2003/0149905 (Santhanam et al.) or Huang et al. Reconsideration is respectfully requested.

### *35 USC Section 103 Rejections*

Claims 1-16 were rejected under 35 U.S.C. 103(a) as being anticipated by Aoki et al. in view of Shirotori et al. and further in view of Santhanam et al. Applicant respectfully traverses the rejection.

Claim 1, 8, 12 and 15 have been amended to clarify the invention. In particular, independent claims 1, 8, 12 and 15 have been amended to recite:

> supplying clock signals to one or both of said ways *in response to an access mode signal, a HITA signal and a HITB signal* (emphasis added).

Support for the amendments in general is provided at least at paragraphs **[0019], [0023]** and paragraph **[0024]**, and more specifically, at paragraph **[0024],** lines 7-10; and shown at least in FIG. 1 at references **24A**, **HITA**, **24B** , **HITB** and **20** of the published application (i.e., U.S. Patent Application Publication No. US 2005/0108480. Therefore, it is respectfully submitted that the amendments raise no question of new matter.

Aoki et al. discloses a set-associative cache memory having a built-in set prediction array is disclosed.[1] In particular, Aoki et al. discloses the information stored in memory array **21** may be accessed by an effective address **20**.[2] Further, Aoki et al. discloses the effective address **20** includes a tag field, a line index field, and a byte field.[3] Furthermore, Aoki et al. discloses the tag field of the effective address **20** is utilized to provide cache "hit" information.[4] Moreover, Aoki et al. discloses the line index field of effective address **20** is utilized to select a specific cache line within memory array **21**, and the byte field of effective address **20** is utilized to index a specific byte within the selected cache line.[5]

In addition, Aoki et al. discloses a match between a tag from one of two ways in directory **22** and the real page number implies a cache "hit." Further, Aoki et al. discloses that the cache "hit" signal (i.e., Sel_0 or Sel_1) is also sent to a set-select multiplexor **25** to select an output from one of the two ways of memory array **21**.

However, Aoki et al. nowhere discloses, as recited in independent claims 1, 8, 12 and 15:

> supplying clock signals to one or both of said ways *in response to an access mode signal, a HITA signal and a HITB signal* (emphasis added).

That is, Aoki et al. nowhere discloses a supplying clock signals to one or both of said ways in response to an access mode signal, a HITA signal and a HITB signal, as recited in claims 1, 8, 12 and 15. In fact, the outstanding Office Action acknowledges deficiencies in Aoki et al. and attempts to overcome these deficiencies with Shirotori et al.[6] However, Shirotori et al. cannot overcome the deficiencies of Aoki et al., as discussed below.

Shirotori et al. discloses a cache memory that automatically sets a low-, semi-, or high-speed mode of operation according to the result of a comparison between a half-period of a reference clock signal and a pulse width of a reference pulse signal provided by a reference pulse

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[1] Aoki et al. at ABSTRACT.
[2] *Id.* at FIG. 2; and column 3, lines 5-6.
[3] *Id.* at FIG. 2; and column 3, lines 6-7.
[4] *Id.* at FIG. 2; and column 3, lines 7-9.
[5] *Id.* at FIG. 2; and column 3, lines 9-14.
[6] Outstanding Office Action at page 3, paragraph 6, lines 14-15.

signal generator.[7] In particular, Shirotori et al. discloses according to the start signal from the start signal generator **7** and the hit information from the hit controller **4**, the access controller **8** supplies an enable signal for allowing the reading of data out of one of the data memories **2** that is associated with the hit tag memory **1**.[8] More specifically, Shirotori et al. discloses, upon receiving the hit information, the access controller **8** *stops immediately supplying the enable signal to the data memories* except to the one associated with the hit tag memory **1** so that only the hit data memory **2** is read (emphasis added).[9]

However, Shirotori et al. nowhere discloses, as recited in independent claims 1, 8, 12 and 15:

> supplying clock signals to one or both of said ways *in response to an access mode signal, a HITA signal and a HITB signal* (emphasis added).

That is, Shirotori et al. nowhere discloses supplying clock signals to one or both of said ways in response to an access mode signal, a HITA signal and a HITB signal, as recited in claims 1, 8, 12 and 15. In particular, Shirotori et al. nowhere discloses all three signals (i.e., "access mode," "HITA" and "HITB") as directly connected to a clock circuit. Thus, Shirotori et al. cannot be used to overcome the deficiencies of Aoki et al.

Therefore, it is respectfully submitted that neither Aoki et al. nor Shirotori et al., whether taken alone or in combination, disclose, suggest or make obvious the claimed invention and that claims 1, 8, 12 and 15, and claims dependent thereon, patentably distinguish thereover.

In fact, the outstanding Office Action acknowledges deficiencies in Aoki et al. and Shirotori et al. and attempts to overcome these deficiencies with Santhanam et al.[10] However, Santhanam et al. cannot overcome all of the deficiencies of Aoki et al. and Shirotori et al., as discussed below.

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[7] Shirotori et al. at ABSTRACT.
[8] *Id.* at FIG. 3; and column 4, lines 61-65.
[9] *Id.* at FIG. 3; and column 5, lines 4-7.
[10] Outstanding Office Action at page 5, paragraph 6, lines 37-38.

Santhanam et al. discloses a processor may include an execution circuit, an issue circuit coupled to the execution circuit, and a clock tree for clocking circuitry in the processor.[11] In particular, Santhanam et al. discloses a data cache **30** may be a circuit with multiple subcircuits (e.g. cache banks) that may be conditionally clocked individually dependent on which bank is accessed by a given load/store instruction.[12] Further, Santhanam et al. discloses the cache banks may be collectively clocked dependent on whether or not a load/store instruction has been issued and has not reached the cache access stage.[13]

However, Santhanam et al. nowhere discloses, as recited in independent claims 1, 8, 12 and 15:

> supplying clock signals to one or both of said ways *in response to an access mode signal, a HITA signal and a HITB signal* (emphasis added).

That is, Santhanam et al. nowhere discloses supplying clock signals to one or both of said ways in response to an access mode signal, a HITA signal and a HITB signal, as recited in claims 1, 8, 12 and 15. Thus, Santhanam et al. cannot be used to overcome the deficiencies of Aoki et al. and Shirotori et al.

Therefore, it is respectfully submitted that none of Aoki et al., Shirotori et al. nor Santhanam et al., whether taken alone or in combination, disclose, suggest or make obvious the claimed invention and that claims 1, 8, 12 and 15, and claims dependent thereon, patentably distinguish thereover.

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[11] Santhanam et al. at ABSTRACT.
[12] *Id.* at FIG. 1; paragraph **[0058]**; lines 4-7.
[13] *Id.* at FIG. 1; paragraph **[0058]**; lines 7-10.

## *Conclusion*

Applicant believes no fee is due with this response. However, if a fee is due, please charge Deposit Account No. 50-0563, under Order No. 20421-00071-US from which the undersigned is authorized to draw.

Dated: February 16, 2007

Respectfully submitted,

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